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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,659	03/18/2004	Jos Manuel Accapadi	AUS920031016US1	6003
35525	7590	11/26/2007		
IBM CORP (YA) C/O YEE & ASSOCIATES PC P.O. BOX 802333 DALLAS, TX 75380			EXAMINER ZHE, MENG YAO	
			ART UNIT 2195	PAPER NUMBER
			MAIL DATE 11/26/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary

Application No.

10/803,659

Applicant(s)

ACCAPADI ET AL.

Examiner

MengYao Zhe

Art Unit

2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>3/18/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1, 7, 8, 10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a useful, concrete and tangible result.

As per claim 1, no physical transformation is recited and additionally, the final result of the claim is merely performing a search for an idle processor, while nothing is being done about the search result—no thread, for example, gets executed as result of the search. Thus the result is not useful.

As per claims 7, 8, and 10, only attempts at a thread steal were made, and so in the situation that the attempts are unsuccessful, nothing happens, making the entire result not tangible and not concrete.

4. Claims 13-16 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are directed to a signal directly or indirectly by claiming a medium and the Specification found in paragraph 88 recites evidence where the computer readable medium is define as a "radio frequency and light wave". In that event, the claims are directed to a form of energy which at present the office feels does not fall into a category of invention. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101.

<http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf>

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-10, 11-12, 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following claim languages are unclear and indefinite:

i) Claim 1, it is uncertain how "a plurality of processors" in lines 1-2 are related to "a plurality of multi-processor modules" in line 3 <i.e. Does each of the multi-processor module contain a plurality of processors?>.

Lines 6-7, it is unclear how the step of "identifying the first thread..." is performed <i.e. Is there an ID for each thread which points to the process that spawned the thread?>.

Line 10, it is not clearly understood as to what is meant for a processor module to be "associated with the existing process" <i.e. does it mean that the invention only picks out a processor that had previously ran a process which spawned the thread? Or a processor that is currently executing a different thread of the same process?>.

ii) Claim 2, it is uncertain how "a queue" is related to a multi-processor module and its processors <i.e. Does each module get its own queue, and each processor within the module get a different queue?>

iii) Claim 7, line 9, it is ambiguous how "failure" happened when the first stealing attempt is made <i.e. Does failure always happen? What triggered the failure? Is it because the process that was the victim of the stealing ran out of threads to steal from?>

It is unclear how "a dedicated queue" of line 11 is different from "a local run queue" of line 6 <i.e. does each module get its own queue, and all the processors within each module get its separate queue as well?>.

iv) Claim 8, it is uncertain as to what "a criterion" might be <i.e. what is it?>.

iv) Claim 11, it is not clearly understood how the steps of "reassigning" in line 9 is related to "comparing a thread load" of line 5 <i.e. does reassigning happen as result of the comparison? For example, if the thread load of one queue is greater than the other, the reassigning happens?>

Claim 15 has the same deficiencies as claim 11 above.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3, 5-6, 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Willen et al., Pub No. 2004/0054999 (hereafter Willen).

9. As per claim 1, Willen teaches a method of queuing threads among a plurality of processors in a multiple processor system having a plurality of multi-processor modules (Para 100, lines 1-3; Para 146, lines 1-15), the method comprising the computer implemented steps of:

receiving a first thread to be processed; identifying the first thread as part of an existing process (Para 61, lines 5-10; Para 62, lines 1-2; Para 161, lines 5-10);

performing a search for an idle processor, wherein the search is restricted to processors of a first multi-processor module associated with the existing process (Para 68, last 2 lines; Para 99, 13-16; Para 144, lines 4-6; Column 146, lines 4-15; Para 147, lines 1-6; Para 161, lines 5-10: Applications or data-sharing groups are restricted to groups of processors, hence, their threads are restricted as well.).

10. As per claims 2, 13, Willen teaches assigning the first thread to a queue dedicated to the first multi-processor module (Para 99, lines 14-16; Para 161, lines 8-10; The switching queue corresponds to the queue for multi-processor module.).

11. As per claim 3, Willen teaches identifying the first multi-processor module as associated with the existing process (Para 99, lines 14-16; Para 144, lines 4-6; Para 146, lines 5-15).

12. As per claim 5, Willen teaches identifying one of the processors as an idle processor; and assigning the first thread to a local run queue associated with the idle processor (Para 147: the queue of each processor corresponds to the local run queue.).

13. As per claim 6, Willen teaches wherein the step of identifying further comprises: reading attribute information of the first thread (Para 147, lines 1-6).

14. As per claim 14, Willen teaches third instructions for identifying a process associated with the first thread (Column 62, lines 1-3), wherein the second instructions identify threads of the process assigned to the first multi-processor module (Para 161, lines 5-10, lines 17-21).

15. As per claim 15, Willen teaches third instructions for comparing a thread load of the first queue with a thread load of a second queue dedicated to a second multi-processor module of the plurality of multi-processor modules (Para 168, lines 8-11); and

fourth instructions for reassigning the first thread to the second queue (Para 193, lines 6-9).

16. As per claim 16, Willen teaches third instructions for reassigning the first thread to a second queue dedicated to a processor of a second multi-processor module of the plurality of multi-processor modules (Para 193, lines 6-9).

17. Claims 7-12, 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimmel et al., Patent No. 6,105,053 (hereafter Kimmel).

18. As per claim 7, Kimmel teaches a method of load balancing in a multiple processor system having a plurality of multi-processor modules (Fig 1A, units 10, 11, 12; Fig 1B, units 110, 111), the method comprising the computer implemented steps of:

performing, by an idle processor of a first multi-processor module, a first attempt at a thread steal from a local run queue of a processor located on the first multi-processor module for reassignment of a thread to a local run queue of the idle processor (Column 11: lines 21-27: stealing within a module);

responsive to failure of the first attempt, performing a second attempt at a thread steal from a dedicated queue associated with a second multi-processor module (Column 10, lines 60-63; Column 11, lines 27-40: stealing amongst modules).

19. As per claim 8, Kimmel teaches evaluating a criterion associated with the second multi-processor module; and responsive to evaluating the criterion, determining if a thread is to be reassigned from the dedicated queue to the local run queue of the idle processor (Column 11, lines 25-40).

20. As per claims 9, 17, Kimmel teaches reassigning a thread of the dedicated queue to the local run queue of the idle processor (Column 11, lines 1-6).

21. As per claim 10, Kimmel teaches responsive to failure of the second attempt, performing a third attempt at a thread steal from a local run queue associated with a processor of the second multi-processor module for reassignment of a thread to the local run queue of the idle processor (Column 10, lines 60-63; Column 11, lines 27-40).

22. As per claim 11, Kimmel teaches a method of load balancing processors in a multiple processor system having a plurality of multi-processor modules, the method

comprising the computer implemented steps of; comparing a thread load of a first queue dedicated to a first multi-processor module with a thread load of a second queue dedicated to a second multi-processor module; and reassigning a thread of the first queue to the second queue (Column 3, lines 5-7; Column 17, lines 46-60).

23. As per claim 12, Kimmel teaches wherein the step of comparing further comprises: determining a difference between the thread load of the first queue and the thread load of the second queue, reassigning the thread responsive to evaluating the difference as greater than a threshold (Column 17, lines 46-60).

24. As per claim 18, Kimmel teaches wherein the first multi-processor module comprises a plurality of central processing units disposed on a first chip, and the second multi-processor module comprises a plurality of central processing units disposed on a second chip (Column 4, lines 17-30).

25. As per claim 19, Kimmel teaches wherein the first multi-processor module is a simultaneous multi-threading central processing unit, and the second multi-processor module is a simultaneous multi-threading central processing unit (Column 5, lines 15-20).

26. As per claim 20, Kimmel teaches wherein the scheduler identifies a second thread of a process associated with the first thread, and the second thread is assigned to the queue (Column 2, lines 36-41; Column 11, lines 1-6).

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

28. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Willen et al., Pub No. 2004/0054999 (hereafter Willen).

29. As per claim 4, Willen teaches being able to identify threads having the same processes (Para 61, lines 5-10; Para 62, lines 1-2; Para 161, lines 5-10) and furthermore, Willen teaches that the user or the system can specify which processor is to be used for executing an application or data-sharing group (Para 144, 146); But Willen does not specifically teaches wherein the step of identifying the first multi-processor module further comprises: maintaining a record of processes having threads

executed by a processor of the first multi-processor module during a predetermined preceding interval.

However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to see that in order for Willen's invention to keep track which processor must be used to execute an application, there must be a record that records processes executed by a processor.

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MengYao Zhe whose telephone number is 571-272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached at 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business

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Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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